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The Xilinx Virtex-5 FXT device provides a tightly coupled integration of processor subsystem, DSP-enabled FPGA fabric, and high-speed communication. Such high levels of integration have allowed both the hardware and software elements of the LTE baseband reference system to be integrated on a single Xilinx FX70T part using standard hardware boards.

Implementing LTE on FPGAs | EE Times

Here's a review of the LTE algorithms and a practical implementation on a Xilinx FPGA. The reference design is tested using multiple video stream with varying encoding rates. By Rob Payne, Xilinx dspdesignline.com (February 06, 2009) The next generation of the 3GPP wireless standard is called long-term evolution (LTE). It provides a leap in performance and a complete move to packet-based processing.

Implementing LTE on FPGAs - Design And Reuse

This paper presents the design and implementation of the LTE-A downlink transmitter and receiver using a Field Programmable Gate Array (FPGA) according to release 10/11 on Virtex 6 XC6VLX240T FPGA...

(PDF) FPGA Implementation of LTE-Advanced Downlink ...

The paper presents an implementation of a 3GPP TS 36.212 LTE turbo decoder. The design of the turbo decoder has been optimized to achieve efficient FPGA resource utilization. This design can be useful for applications, which is critical to resource utilizations, but do not need high throughput

FPGA implementation of LTE turbo decoder using MAX-log MAP ...

Learn how to model LTE wireless functionality for FPGA implementation, along with a connected workflow from algorithm design to targeting a Xilinx® Zynq®-based software-defined radio From Wireless Standard to Software Defined Radio: An FPGA implementation of an LTE design Video - MATLAB

From Wireless Standard to Software Defined Radio: An FPGA ...

Overview of LTE standard (training sequences, LTE resource grid) Using real-world recordings to test your design Receiver techniques, such as synchronization, carrier recovery, and equalization

From Wireless Standard to Software Defined Radio: An FPGA ...

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Fpga Implementation Of Lte Downlink Transceiver With

FPGA Implementation of LTE Downlink Transceiver with Synchronization and Equalization Sara M. Hassan Abdelhalim Zekry Modern Academy, Cairo, Egypt Ain Shams University, Cairo, Egypt ABSTRACT Long Term Evolution (LTE) is an advanced standard of the mobile communication systems. LTE has been developed by the 3rd Generation Partnership Project (3GPP).

FPGA Implementation of LTE Downlink Transceiver with ...

In this paper, we have filled this gap of unavailability of actual hardware implementation of a UFMC transmitter. Hence, first real time FPGA implementation of UFMC transmitter complying with the timing requirements of 10MHz channelization of LTE is presented here.

FPGA Implementation of UFMC Based Baseband Transmitter ...

This paper presents the FPGA (Field Programmable Gate Array) implementation simulation results for Turbo encoder and decoder structure for 3GPP-LTE standard. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2. List of the following materials will be included with the Downloaded Backup: 1.

Design and Implementation of Turbo Coder for LTE on FPGA

This is an overview on LTE implementation using XILINX FPGA Graduation Project in arabic aimed at third year students. VHDL was used. This a link to download the presentation used in the video ...

Overview on LTE implementation using XILINX FPGA Graduation Project (Arabic)

The Turbo Decoder in Wireless HDL Toolbox™ is a Simulink® building block for use in FPGA or ASIC designs that need to deliver LTE signal information to your application. Typically, these designs start as algorithms in MATLAB® and LTE Toolbox™. Learn how to use your MATLAB based test environment to drive your Simulink based hardware implementation model and compare the results against your algorithmic golden reference model.

Verifying an FPGA Implementation of an LTE Turbo Decoder ...

Read Free Fpga Implementation Of An Lte Based Ofdm Transceiver For implementation of Turbo Decoder is done on the Field Programmable Gate Array (FPGA), due to its low cost and very short development cycle. The design is coded in the verilog hardware programming language and simulated using Xilinx® simulator of version 14.2 and

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developed to design SoC on a heterogeneous FPGA-CPU platform on the basis of performance metrics such as area, power, and latency. Design of physical downlink shared channel (PDSCH) in long-term evolution (LTE) is presented as a case study. This paper provides the implementation of the transmitter

Automated performance-based design technique for an ...

In order to support high-definition video transmission, an implementation of video transmission system based on Long Term Evolution is designed. This system is developed on Xilinx Virtex-6 FPGA...

FPGA Implementation of Video Transmission System Based on LTE

Implementation of an efficient turbo decoder with low complexity, short delay and insignificant performance degradation is currently a quite challenging task. The paper presents an implementation of a 3GPP TS 36.212 LTE turbo decoder. The design of the turbo decoder has been optimized to achieve efficient FPGA resource utilization.

FPGA implementation of LTE turbo decoder using MAX-log MAP ...

FPGA Implementation of Turbo Decoder for LTE Standard . By S. Rajaram, A. Sakthi Amutha Vardhini and K. Kalyani. Abstract. The data rate of 100 Mbps will be supported by upcoming 3G Long Term Evolution (LTE) standard. In 20 MHz of bandwidth, this data rate will be attained. For the arrival of high data rate of the 3G LTE systems, there is an ...

FPGA Implementation of Turbo Decoder for LTE Standard - CORE

Abstract This paper describes the implementation on field programmable gate array (FPGA) of a turbo decoder for 3GPP Long-Term Evolution standard. Considering the high data rates required by this standard, parallel decoding architecture is used.

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