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Additional information on the models, ports, and options can be obtained from UG196, Virtex-5 FPGA RocketIO GTP Transceiver User Guide. Additional information regarding the Quantum Channel Designer can be obtained from the SiSoft Quantum Channel Designer User Guide (provided with the SIS Kit installation). Page 8: Installation And Requirements

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Chapter 1: Added "Clock Gating for Power Savings" on page 22 . Revised Figure 1-2, page 26 . Revised Figure 1-16, page 33. Chapter 2: Revised DCM reset and locking process in "Reset Input - RST," page 49 . Updated DO[2] description in Table 2-4, page 52.

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For 3.3V I/O operation, refer to UG190: Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines. 5. For more flexibility in specific designs, a maximum of 100 user I/Os can be stressed beyond the normal specification for no more than 20% of a data period .

Virtex-5 FPGA Data Sheet: DC and Switching Characteristics ...

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The LUTs in Virtex-5 FPGAs can be configured as either 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Four such LUTs and four flip flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a Configurable Logic Block (CLB).

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